Single phase Cascaded H-Bridge Multilevel Inverter study and comparison of different levels

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Abstract:

Multi-level inverter used in applications that require high power and medium voltage. It can be used in: homes, factories, as well as in the military and medical aspects. This paper deals with study of Cascaded H-bridge and comparison between different levels for this type (three level, five level and seven level are presenting in this study). The comparison based on the design, the cost and the total harmonic distortion. The design tends to be more complicated when increasing the number of levels because of using more sources, more H-bridges and more connection wires. The control becomes more complexity as well as the inverter will be expensive and heavy as compared to low levels. Considering to the results of Matlab\ Simulink which illustrate the total harmonic distortion is being low when increasing the level and this will be an important matter in the output voltage. The level number of multi-level inverter is choosing according to the type of load.

Key words: Cascaded H-Bridge multilevel inverter, Sinusoidal pulse width modulation techniques

عاكس متعدد المستويات قنطرة H تتالي احادي الطور دراسة ومقارنة المستويات المختلفة

الخلاصة:

العاكس متعدد المستويات (Multilevel Inverter) يستخدم في التطبيقات التي تتطلب قدرة عالية وفولتية متوسطة. يمكن استخدامه في المنازل, المصانع, كذلك في الجوانب الطبية والعسكرية.هذا البحث يختص بدراسة العاكس متعدد المستويات نوع Cascaded H-Bridge ومقارنة بين مستويات مختلفة لهذا النوع (ثلاث, خمس وسبعة مستويات). المقارنة اعتمدت على التصيم , الكلفة والتشوه التوافقي الكلي (Total Harmonic Distortion). التصميم يكون اكثر تعقيداً عند زيادة عدد المستويات بسبب استخدام مصادر, خلية H-bridge وتوصيلات اكثر. التحكم بالمفاتيح اكثر صعوبة عند زيادة عدد المستويات كذلك العاكس يصبح مُكلف واثقل بالمقارنة مع المستوي الاقل. بالنظر الى نتائج Matlab التي توضح التشوه التوافقي الكلي (Total Harmonic Distortion) يكون اقل عند زيادة المستوى وهذا امر مهم في موجة الفولتية الخارجة. مستوى العاكس متعدد المستويات (Multilevel Inverter) يختار حسب نوع الحمل.

الكلمات المفتاحية: العاكس متعدد المستويات نوع Cascaded H-Bridge, مستوى العاكس متعدد المستويات

I. Introduction:

Development of the industries has led to increased need for using high power equipment in megawatts level. For purpose of providing energy to this equipment the multilevel inverter appeared. Multilevel inverter is a device which converts Direct Voltage Source (DCV) to Alternating Voltage Source (ACV). It consists of a group of semiconductor and generates stepped voltage with staircase waveform. Increasing the number of steps lead to smooth signal with reduces distortion and the shape of the wave approaching to sine wave. There are many power applications need multilevel inverter such as variable speed drive, flexible AC transmission systems (FACTS) and renewable energy such as wind, full cells and photovoltaic [1,2]. There are different topologies of multilevel inverter: Neutral point clamped multilevel inverter or Diode clamped multilevel inverter [3,4], Fly capacitance

multilevel inverter and Cascaded H-bridge multilevel inverter [5,6]. Neutral point clamped multilevel inverter and Fly capacitance multilevel inverter are single DC source but Cascaded H-bridge multilevel inverter uses multi DC source. Cascaded H-bridge multilevel inverter preferably employ instead of the other two types because it's required less number of components but also need separate DC source in each level [7]. The multilevel inverter obtains an alternating current output voltage with a staircase waveform [8].

The main features of multi-level inverter are:[9]

1. Less distortion and lower dv/dt of output voltage.
2. Minimum distortion of input current.
3. They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
4. Operate with low switching frequency, which reduce switching loss.

Multilevel inverter circuits have been appearing for more than 30 years. First appeared in 1975.[10]

II. Cascaded H Bridge Multilevel Inverter (CHBMLI)

The set of H-Bridge (Full Bridge) inverter with separate DC Sources are connected in cascade to configure the cascaded H-Bridge multilevel inverter [11]. Figure (1) shows the circuit diagram of an n level inverter. The output voltage generates by each single H-bridge of an inverter have three different value of voltage: $+V_{DC}$, 0 and $-V_{DC}$. The output voltage generated by cascade H-Bridge inverter is the total voltage generated by each H-bridge cell [12].The required number of semiconductor switches are 2(n-1) where n is the number of level. The number of DC sources is equal to the number of H-Bridge cells. The cost and the weight of this inverter is less than Diode clamped multilevel inverter and Flying Capacitor multilevel inverter but the losses of it are more as compared with the other two types [13]. The voltage unbalance of H-bridge multilevel inverter is very low. It can be used in many applications such as motor drive system, photovoltaic cell, solar and fuel cell.

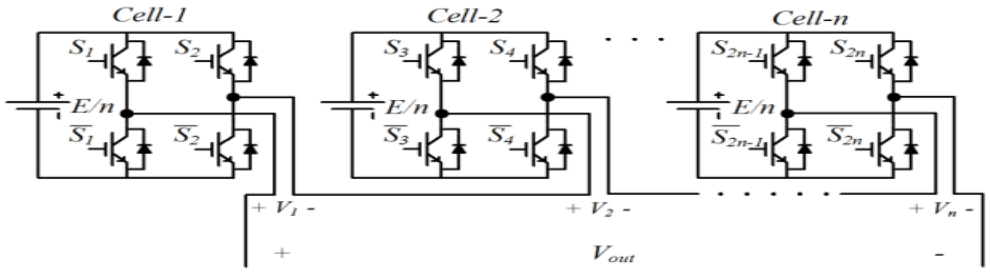

Figure (1). Circuit diagram of an n level inverter [12]

i. Single phase three level CHBMLI

Figure (2) shows the circuit of single phase three level CHBMLI. The circuit consisting of single DC source and four switches (single H-bridge cell). The waveform of output voltage of this level is shown in figure (3). The three levels are + V_{DC}, 0 and -V_{DC}. Different operation cases of three level CHB inverter are explained below in table1.

Table1. Switches status of three level CHBMLI [14]

Case	Output voltage	S_1	S_2	S_3	S_4
1	0	1	0	1	0
2	+V_{DC}	1	0	0	1
3	0	0	1	0	1
4	- V_{DC}	0	1	1	0

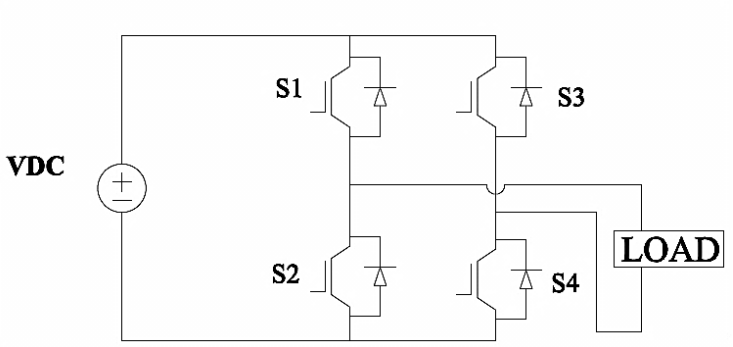

Figure (2). Circuit of single phase three level CHBMLI [14]

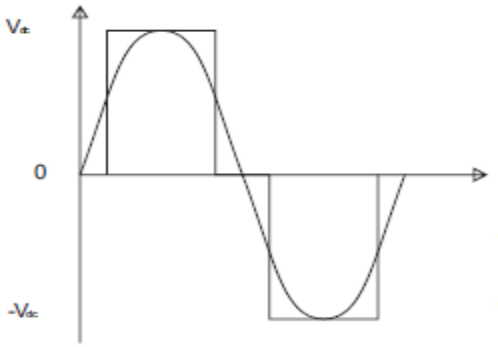

Figure (3). Output voltage waveform of three level CHBMLI [14]

ii. Single phase five level CHBMLI

Figure (4) shows the circuit of single phase five level CHBMLI. The circuit consisting of dual DC sources and eight switches (two H-Bridge cells). The output voltage of five level inverter is generated by two H-bridge cell. The voltage of the first H-Bridge cell is V_1 and the second H-Bridge cell is V_2. The total voltage of five level inverter is the sum of V_1 and V_2. Figure (5) shows the waveform of output voltage of this level. The five levels are 0, $+V_{DC}$, $+2\ V_{DC}$, $-V_{DC}$ and $-2V_{DC}$. Different operation cases of five level CHB inverter are explained below in table2.

Table2. Switches status of five level CHBMLI [14]

Case	Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	0	1	0	1	0	1	0	1	0
2	$+V_{DC}$	1	0	0	1	1	0	1	0
3	$+2V_{DC}$	1	0	0	1	1	0	0	1
4	$+V_{DC}$	1	0	1	0	1	0	0	1
5	0	0	1	0	1	1	0	1	0
6	$-V_{DC}$	0	1	0	1	0	1	1	0
7	$-2V_{DC}$	0	1	1	0	0	1	1	0
8	$-V_{DC}$	0	1	1	0	0	1	0	1

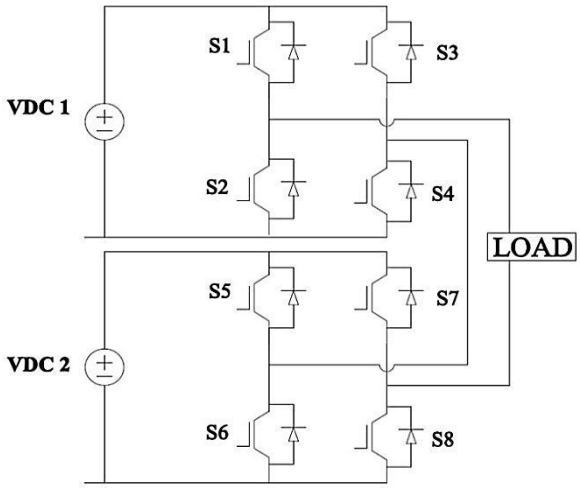

Figure (4). Circuit of single phase five level CHBMLI [14]

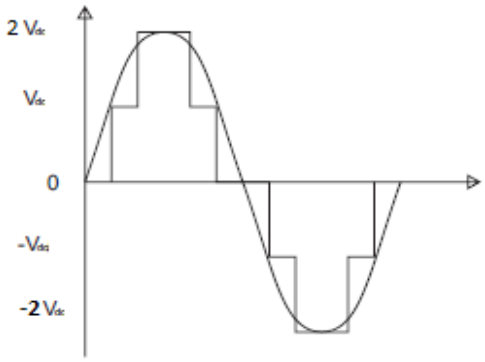

Figure (5). Output voltage waveform of five level CHBMLI [14]

iii. Single phase seven level CHBMLI

Figure (6) shows the circuit of single phase seven level CHBMLI. The circuit consisting of twelve switches (three H-Bridge cells) and three DC sources**.** The waveform of output voltage of seven level multilevel inverter is shown in figure (7). The seven levels are 0,+ V_{DC}, +2 V_{DC}, ,+3 V_{DC}, - V_{DC} , -2 V_{DC} and -3 V_{DC}. Different operation cases of seven level CHB inverter are explained in table3.

Table 3. Switches status of seven level CHBMLI [14]

Case	Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
1	0	1	0	1	0	1	0	1	0	1	0	1	0
2	$+V_{DC}$	1	0	0	1	1	0	1	0	1	0	1	0
3	$+2V_{DC}$	1	0	0	1	1	0	0	1	1	0	1	0
4	$+3V_{DC}$	1	0	0	1	1	0	0	1	1	0	0	1
5	$+2V_{DC}$	0	1	0	1	1	0	0	1	1	0	0	1
6	$+V_{DC}$	0	1	0	1	0	1	0	1	1	0	0	1
7	0	0	1	0	1	0	1	0	1	0	1	0	1
8	$-V_{DC}$	0	1	1	0	0	1	0	1	0	1	0	1
9	$-2V_{DC}$	0	1	1	0	0	1	1	0	0	1	0	1
10	$-3V_{DC}$	0	1	1	0	0	1	1	0	0	1	1	0
11	$-2V_{DC}$	0	1	0	1	0	1	1	0	0	1	1	0
12	$-V_{DC}$	0	1	0	1	0	1	0	1	0	1	1	0

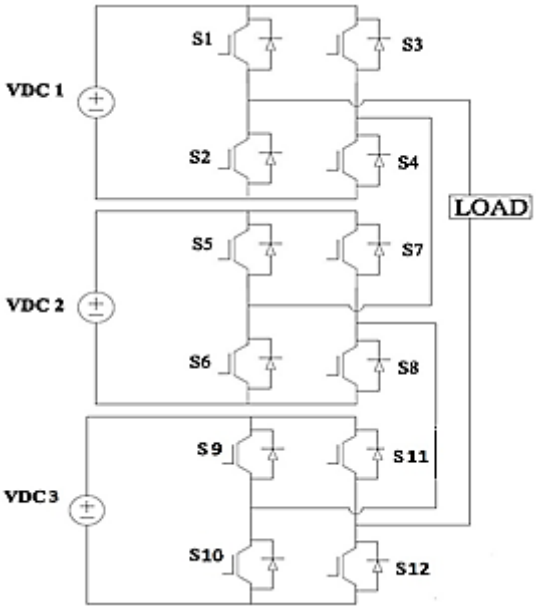

Figure (6). Circuit of seven level CHBMLI [14]

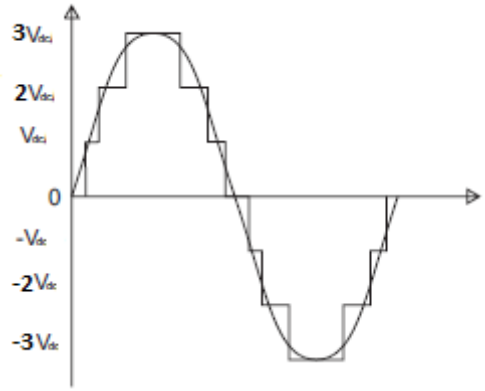

Figure (7). Output voltage waveform of seven level CHBMLI [14]

Table 4. Comparison between three level, five level and seven level of CHBMLI / phase

Parameters	Three level	Five level	Seven level
Number of cells	1	2	3
Number of switches	4	8	12
THD	52.23%	26.63%	18.01%
Cost	Less	Medium	More
Weight	Less	Medium	More

III. Sinusoidal PWM techniques (SPWM)

Different multicarrier techniques are used to decrease the distortion of multilevel inverter [15]. SPWM is one of these techniques, the sinusoidal wave is a modulating signal and the triangular waves are carrier signals. An n level inverter need (n-1) carrier signal [16]. The pulses of gates are generated as a result of comparing a sinusoidal modulating signal with a triangular carrier signals. Figures (8, 9 and 10) Shows carrier signals with a reference modulating signal of three, five and seven level CHB inverter respectively. The carrier signals are in the same phase and amplitude but different from each other in the dc level [17]. The main advantage of this technique is decreasing the size of the filter to minimum and therefore reduces the cost, size and weight of an inverter.

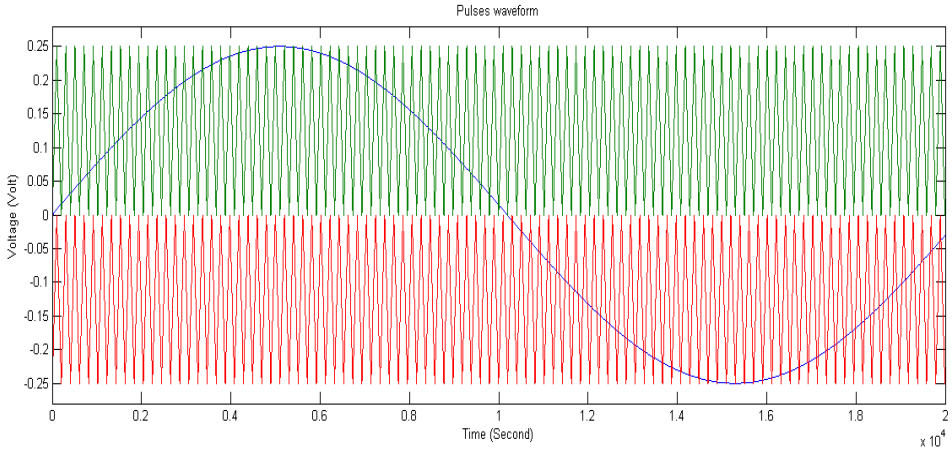

Figure (8). Carrier and Reference signals of three level CHBMLI

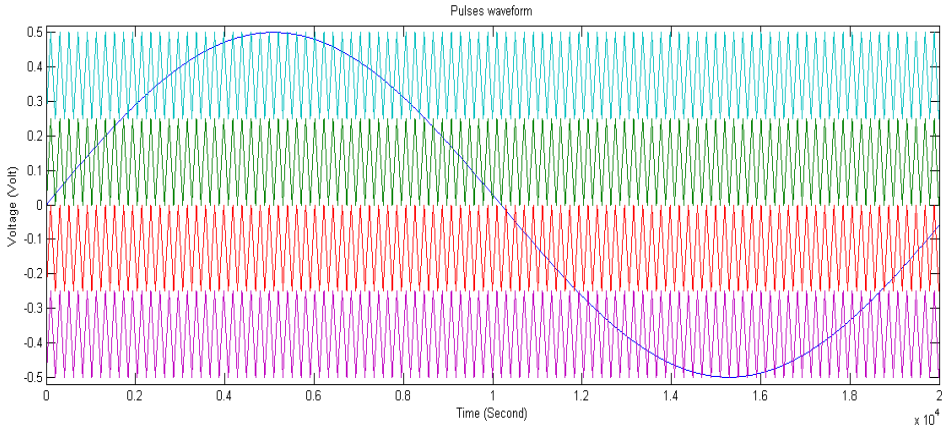

Figure (9). Carrier and Reference signals of five level CHBMLI

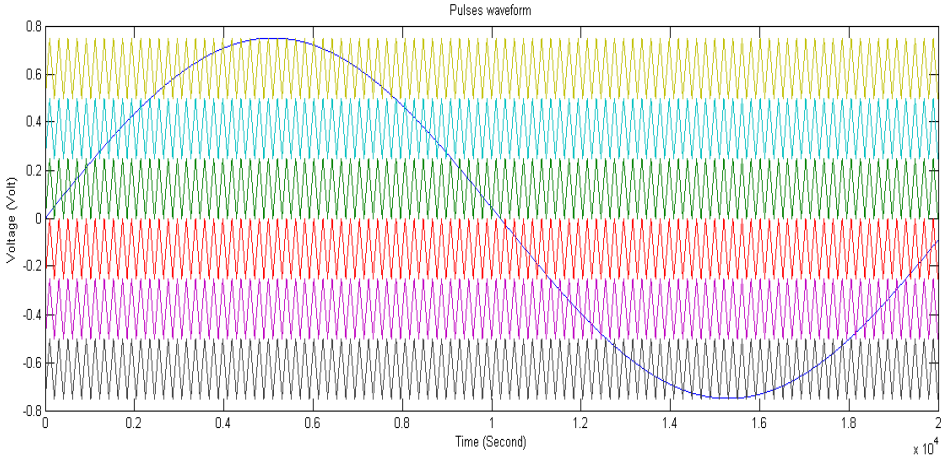

Figure (10). Carrier and Reference signals of seven level CHBMLI

V. Results:

Design of CHBMLI and the results of output voltage waveforms, output current waveforms and values of THD are obtained by Matlab\ Simulink 2010 version 7.11.0. The figures below show the results of three, five and seven level respectively with resistive and inductive load (R=100Ω and L=0.5H).

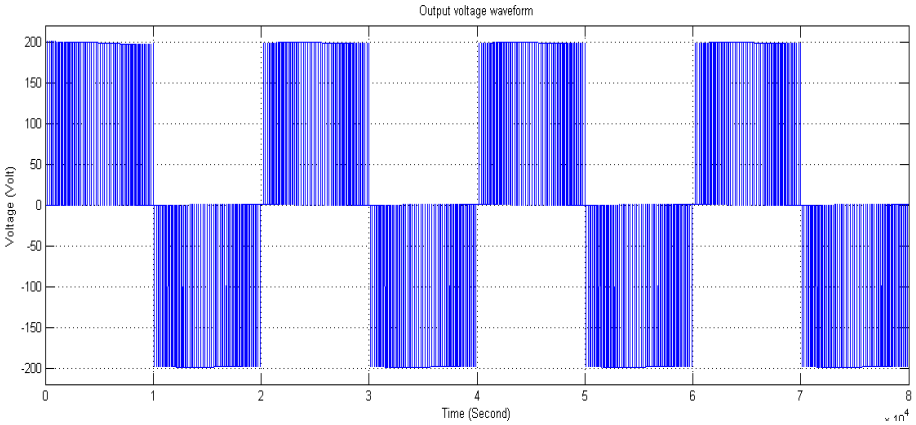

Figure (11). Output voltage waveform of three level

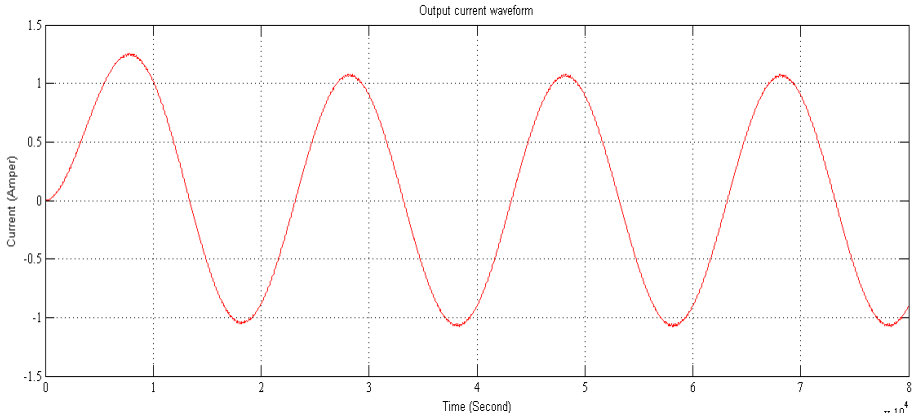

Figure (12). Output current waveform of three level

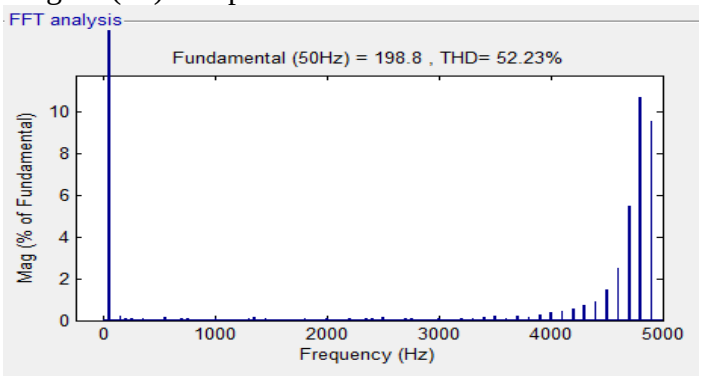

Figure (13). THD of three level

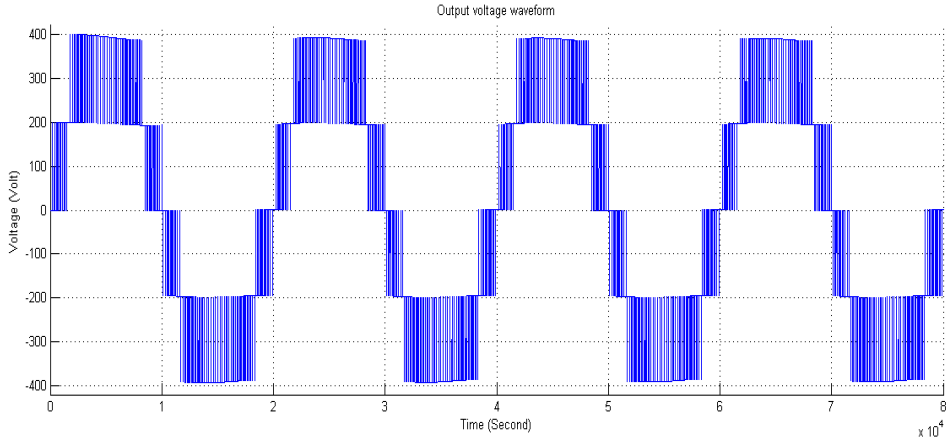

Figure (14). Output voltage waveform of five level

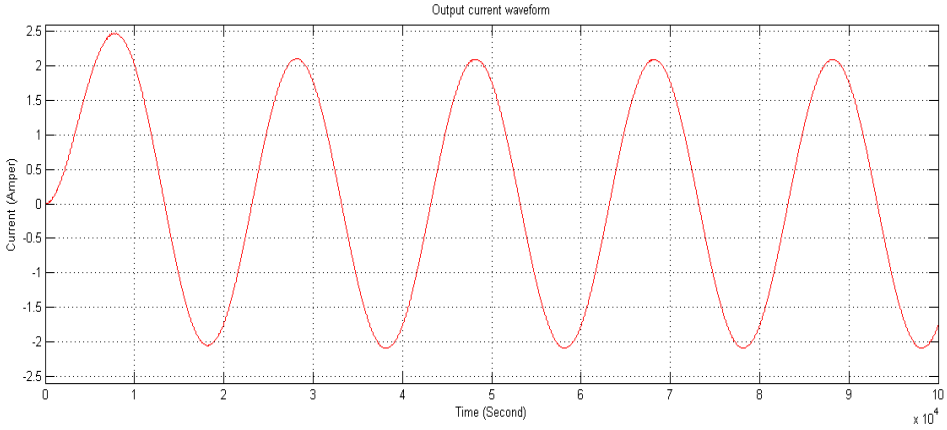

Figure (15). Output current waveform of five level

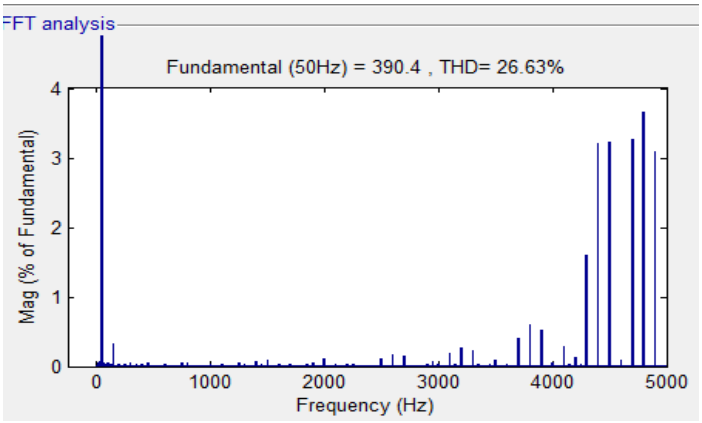

Figure (16). THD of five level

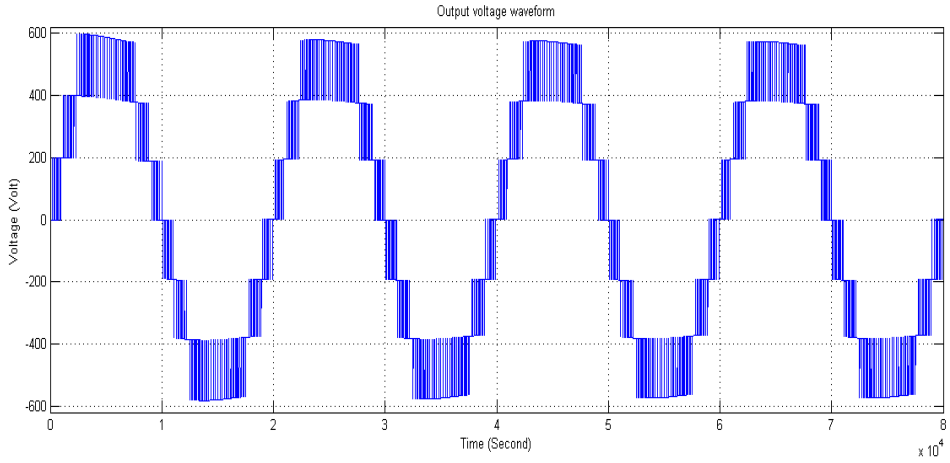

Figure (17). Output voltage waveform of seven level

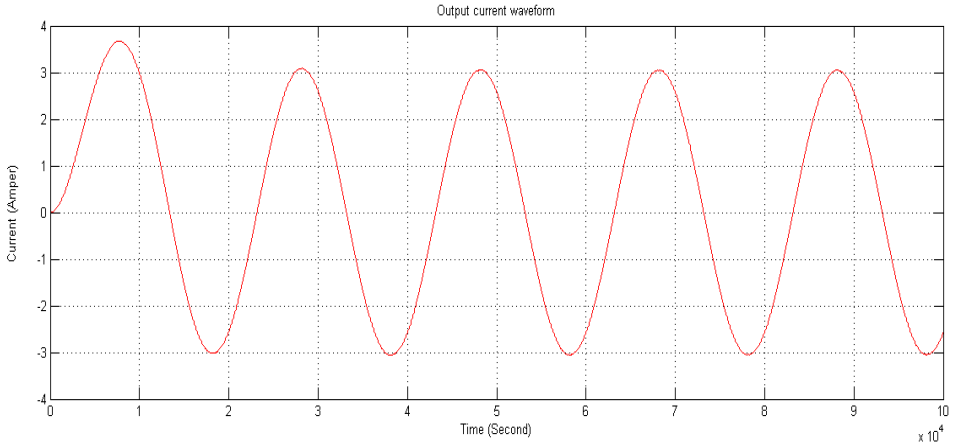

Figure (18). Output current waveform of seven level

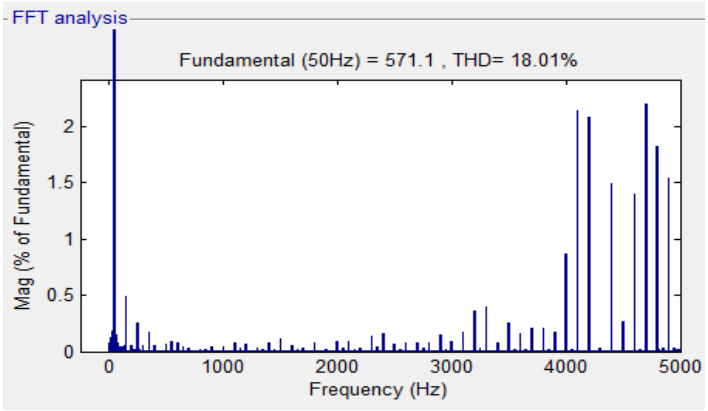

Figure (19). THD of seven level

V. Conclusion:

This paper deals with the study and comparison of cascaded H-Bridge topology with different levels. The comparison has three different level three, five and seven level and the method of control which use is SPWM. The result of MATLAB\Simulink appears less distortion at high level i.e. total harmonic distortion (THD) decreases with the increase in the number of level. The output voltage waveform of high level is improving and approaching more to the sinusoidal waveform. The output current of seven level is more than output currents of five level and three level. These are the advantages of increasing the number of level. But the cost, size and weight are increasing as well as the design is more complicated in high level of Multilevel Inverter.

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