Solar Energy Collector Gain Digital Electronic Meter

Saleim Hachem Farhan Hassan Ali Salman Gailan Abdulkader Institute of Technology Baghdad, Middle Technical University, Al Za'faraniya, Baghdad, Iraq

saleimhachem@yahoo.com

Abstract

This paper introduces the design and theory of a digital meter for measuring the total useful solar energy gain of a flat – plate collector. This is an important parameter of the collector involved in determining the efficiency. Measurement is carried out in term of the collector fluid inlet temperature T_i , the fluid outlet temperature T_o , and the mass flow rate m^* of the working fluid flowing through the collector. Voltages representative of the variable parameters are assessed and processed using a non-linear analog to digital converter (ADC) and voltage to frequency convertor (VFC) to produce a digital number representative of the solar collector gain.

Keywords: solar energy, digital meter, frequency convertor, collectors, electronic meter.

كسب جامع الطاقة الشمسية للمقياس الالكتروني الرقمي

سليم حاجم فرحان حسن علي سلمان كيلان عبد القادر معهد التكنولوجيا بغداد ، الجامعة التقنية الوسطى

الخلاصة

يقدم هذا البحث تصميم ونظرية عداد رقمي لقياس الطاقة الشمسية المفيدة من جامع لوحة مسطحة. وهذا هو العامل المهم من الجامع في تحديد الكفاءة. ويتم القياس من حيث درجة حرارة السائل الداخلية للجامع T_i ، ودرجة حرارة منفذ السائل T_o ، ومعدل التدفق الشامل T_o من السوائل العاملة التي تتدفق من خلال الجامع. ويتم تقييم ومعالجة الفولتية الممثلة للعوامل المتغيرة باستخدام محول تناظري غير خطي الى المحول الرقمي (ADC) ومحول الفولتية الى تردد (VFV) لانتاج رقم رقمي يمثل الكسب لجامع الطاقة الشمسية.

الكلمات المفتاحية: الطاقة الشمسية، العداد الرقمي، محول التردد ، جامع الطاقة، العداد الالكتروني

Introduction

A solar collector is the essential item of equipment which transforms solar radiant energy to some other useful energy form. [1] The principle application of this units are in solar water heating systems, while potential uses include building heating and air conditioning and many domestic requirements. Flat-plate collectors can be designed for applications requiring energy delivering at moderate temperature up to perhaps 100 C° above ambient temperature. Figure (1) shows the basic flat-plate solar energy collector. In order to determine the goodness of the performance and efficiency of the flat

plate collector it is necessary to make available an important parameter. It is the total useful solar energy gain of the collector. It can be written as:[2]

$$Q_u = (m \cdot C_P)(T_0 - T_i)....(1)$$

Where

 $Q_u \longrightarrow$ The total useful energy gain of the collector

m The mass flow rate of the collector working fluid

 $C_P \longrightarrow$ The specific heat of the working fluid

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 T_0 Outlet fluid temperature

 $T_i \longrightarrow$ Inlet fluid temperature

Also we have,

$$m = k \sqrt{\frac{P_S \Delta P}{T_S}} \dots (2)$$

Where,

K _____ a constant

 $P_s \longrightarrow$ Fluid static pressure

 $\Delta P \longrightarrow$ Fluid volumetric flow rate

 $T_s \longrightarrow$ Fluid static temperature

This paper introduces the design and theory of a digital meter for measuring the flat plate solar energy collector gain. Five voltages V_1 , V_2 , V_3 , V_4 and V_5 are developed, via five transducers, representative of T_o , T_i , P_s , ΔP and T_s respectively.

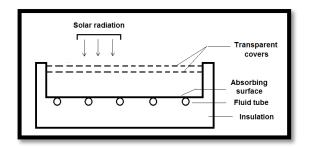


Figure (1) A cross-section of a basic flat plate solar collector.

Those voltages are processed using a nonlinear ADC and VFC to produce digital number representative of the collector gain given in term of voltages by proportionality equation as,

$$Q_u \propto (V_2 - V_1) \sqrt{\frac{V_3 V_4}{V_5}}$$
(3)

Figure (2) shows a block diagram for the transducers arrangement. [3]

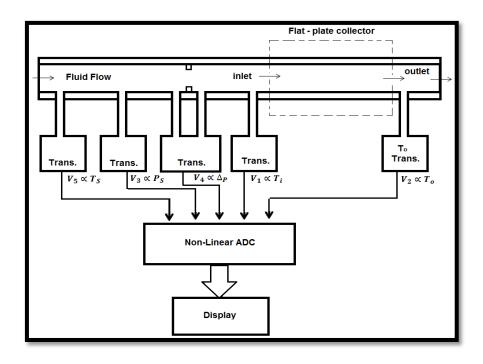


Figure (2) A block diagram of the transducers arrangement of the collector gain meter.

Theory and operation

Figure (3) shows a schematic diagram of the flat- plate solar collector gain meter. At $t=t_o$, the control signal is applied to the system. This signal discharges all the integrating capacitors and also reset the counter to count zero. At first, the voltages (-V5) and V4 are applied to the input of integrators I_1 , and I_2 , respectively. The output of the integrators I_1 is a rampup voltage given by:[4]

$$V_a = \frac{-1}{R_1 C_1} \int_{t_0}^{t} -V_5 dt = \frac{V_5}{R_1 C_1} (t - t_0)...(4)$$

And that of I₂ is,

$$V_b = \frac{-1}{R_2 C_2} \int_{t_0}^{t} -V_4 dt$$
$$= \frac{-V_4}{R_2 C_2} (t - t_0) \dots (5)$$

At $t = t_0$, V_a becomes equal to V_3 .

$$V_a(t_1) = V_3 = \frac{V_5}{R_1 C_1} (t_1 - t_0)$$

$$\therefore t_1 - t_0 = R_1 C_1 \frac{V_3}{V_2} \dots (6)$$

Meanwhile $V_b(t_1)$ is equal to,

$$V_b(t_1) = \frac{-V_4}{R_2 C_2} (t - t_0)$$

$$= \frac{R_1 C_1}{R_2 C_2} \frac{V_3 V_4}{V_5} \dots (7)$$

At this moment a positive reference voltage is applied to the input of the integrator I_1 , while the difference V_a - V_3 is applied to the input of the integrator I_2 .

For $t > t_1$

$$V_{a} = V_{3} - \frac{1}{R_{1}C_{1}} \int_{t_{1}}^{t} V_{r} dt$$

$$= V_3 - \frac{V_r}{R_1 C_1} (t - t_1) \dots (8)$$

And.

$$\begin{split} V_b &= V_b(t_1) - \frac{1}{R_2 C_2} \int_{t_1}^t (V_a - V_3) \, dt \\ &= \frac{R_1 C_1}{R_2 C_2} \frac{V_3 V_4}{V_5} + \frac{1}{R_2 C_2} \int_{t_1}^t \frac{V_r}{R_1 C_1} (t \\ &- t_1) \, dt \\ &= \frac{R_1 C_1}{R_2 C_2} \frac{V_3 V_4}{V_5} + \frac{V_r}{2(R_1 C_1)(R_2 C_2)} (t - t_1)^2 \dots (9) \\ \mathrm{At} &= t_2 \; , \, V_b \; \mathrm{becomes} \; \mathrm{equal} \; \mathrm{to} \; \mathrm{zero}. \\ V_b(t_2) &= 0 = \\ \frac{R_1 C_1}{R_2 C_2} \frac{V_3 V_4}{V_5} + \frac{V_r}{2(R_1 C_1)(R_2 C_2)} (t_2 - t_1)^2 \\ & \therefore t_2 - t_1 = R_1 C_1 \sqrt{\frac{2}{V_r}} \sqrt{\frac{V_3 V_4}{V_5}} \dots (10) \end{split}$$

The counter is allowed to count during the interval $t_2 - t_1$ with a clock frequency, f_0 which is the output frequency of the VFC, given by,[5]

$$f_0 = k_f (V_2 - V_1) \dots (11)$$

Where, k_f is the constant of the conversation and $V_2 - V_1$ is the input voltage of the VFC.

We have

Where, N_{t_2} is the final on the counter at the end of the interval $t_2 - t_1$.

$$k = constant = R_1 C_1 k_f \sqrt{\frac{2}{V_r}}$$

Thus.

 N_{t_2} is proportional to the solar collector gain

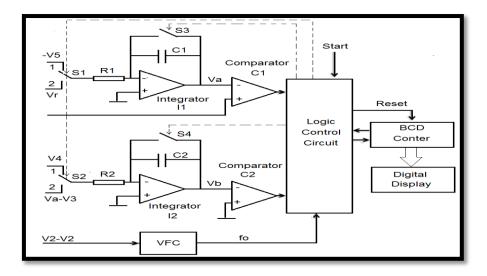


Figure (3) Schematic diagram of the falt- plate solar collector gain digital meter.

Circuit Operation

Figure (4) shows the complete circuit diagram of the solar–collector gain digital meter. Figure 5 shows the timing diagram of the meter.[6]

The start signal is applied at $t=t_o$. this signal closes S_3 and S_4 , momentarily, thus disc arching the capacitors C_1 and C_2 , respectively, also, the counter and the D-flip are reset.[7]

The zero logic of Q switches the SPDT analogue switches S_1 and S_2 to the position

1. The integrator output voltages are given by,

$$V_a = \frac{-1}{R_1 C_1} \int_{t_0}^{t} -V_5 dt = \frac{V_5}{R_1 C_1} (t - t_0) \dots (13)$$

And

$$V_b = \frac{-1}{R_2 c_2} \int_{t_0}^{t} -V_4 dt = \frac{-V_4}{R_2 c_2} (t - t_0)...(14)$$

At $t = t_1$, V_a became equal to V_3 . The output of the capacitor C_1 changes state from high to low logic. This negatively going edge triggers the d-type flip flop, setting Q to logic 1. [8]

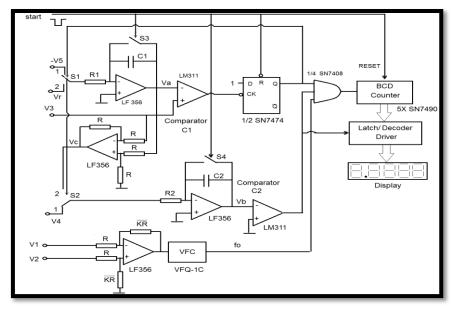


Figure (4) Complete Circuit Diagram of the flat Plat Solar collector gain digital meter

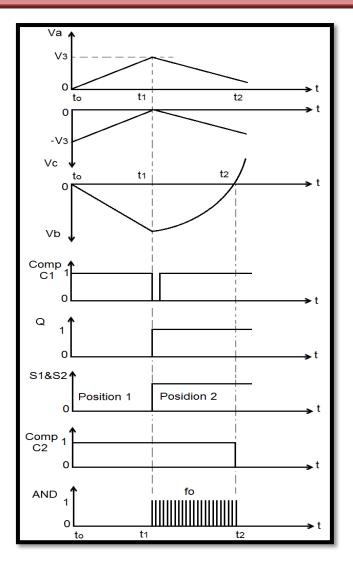


Figure (5) Timing diagram of the flat-plat collector gain digital meter.

The high logic level on Q switches S1 and S2 to position 2. As the output comparator C2 is already high, the high logic level of Q enables the AND gate. The counter starts counting just at $t = t_1$. We have,[9]

$$V_a(t_1) = V_3 = \frac{V_5}{R_1 C_1} (t_1 - t_0) \dots (15)$$

$$\therefore t_1 - t_0 = R_1 C_1 \frac{V_3}{V_5}$$

$$\text{And } V_b(t_1) = \frac{V_4}{R_2 C_2} (t_1 - t_0)$$

$$= \frac{-R_1 C_1}{R_2 C_2} \frac{V_3 V_4}{V_5} \dots (16)$$

For $t > t_1$, we have,

$$V_{a} = V_{a}(t_{1}) - \frac{1}{R_{1}C_{1}} \int_{t_{1}}^{t} V_{r} dt$$

$$= V_{3} - \frac{V_{r}}{R_{1}C_{1}} (t - t_{0}) \dots (17)$$

$$V_b = V_b(t_1) - \frac{1}{R_2 C_2} \int_{t_1}^t V_c \, dt$$

Where

$$V_C = V_a - V_3$$

= $\frac{-V_3}{R_1 C_1} (t - t_0)$ (18)

$$V_b = \frac{R_1 C_1}{R_2 C_2} \frac{V_3 V_4}{V_5} + \frac{V_r}{2(R_1 C_1)(R_2 C_2)} (t - t_1)^2$$

At $t = t_2$, V_b become equal to zero.

$$\begin{split} V_b(t_2) &= 0 = \frac{R_1C_1}{R_2C_2} \frac{V_3V_4}{V_5} \\ &+ \frac{V_r}{2(R_1C_1)(R_2C_2)} (t_2 \\ &- t_1)^2 \end{split}$$

$$\dot{x} t_2 - t_1 = R_1 C_1 \sqrt{\frac{2}{V_r}} \sqrt{\frac{V_3 V_4}{V_5}} \dots (19)$$

The comparator C_2 changes state from high to low. Counting is ceased and the final number on the counter is:[10]

$$N_{t_2} = (t_2 - t_1) f_0 \dots (20)$$

Where,

 N_{t_2} the number on the counter at the end of the interval $t_2 - t_1$.

 F_o is the output frequency of the VFC , given by

$$f_0 = k_f (V_2 - V_1)$$
.....(21)

Where.

 k_f is the conversion constant of the VFC.

Thus,

$$N_{t_2} = R_1 C_1 k_f \sqrt{\frac{2}{V_r}} \sqrt{\frac{V_3 V_4}{V_5}} (V_2 - V_1)$$

$$= k \sqrt{\frac{V_3 V_4}{V_5}} (V_2 - V_1) \dots (22)$$

$$k = R_1 C_1 k_f \sqrt{\frac{2}{V_r}} = constant$$

A proper adjustment of the value of k, N_{t_2} is obviously a representative of the solar energy gain.[11]

Results

The circuit of fig 4 was tested for different values of the inputs. Figure 6 shows linearity of the system with V_3 equals V_4 for different values of V_5 . Figure 7 shows the square routing non-linearity of the system with V_3 equals to V_5 for different values of V_4 . Experimental results an overall error of less than ± 0.5 % as compared to the theoretical ones. Output digital numbers shown in figures 6 and 7 are multiplied by a factor of 2 which may be adjusted in Eq. 19 to be, say, a multiple of 10.

Conclusions

The design of a flat- plate solar collector energy gain digital meter is introduced. Experimental results show an error of less than $\pm~0.5~\%$. the circuit accuracy is mainly affected by the DC offset of the integrators , the speed and the threshold voltage of the comparators, linearity of the VFC and the tolerance of the capacitive components used. However, higher accuracy is expected with carefully selected and adjusted components.

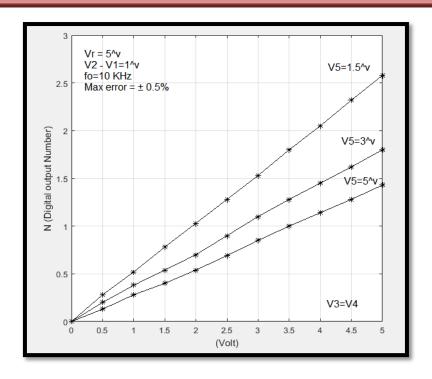


Figure (6) Experimental results of the solar collector gain meter showing its linearity

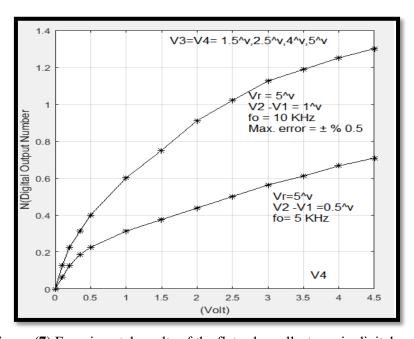


Figure (7) Experimental results of the flat solar collector gain digital meter

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